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-	42	(address near4 requesting) same (program$4 or software or code) same (download$4 or install$4 or upload$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 14:23

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-	51	((customized or specialized) adj code) same (download$3 or install$3 or upload$3 or send$3 or transmit$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 14:27
-	25	((customized or specialized) adj code) same (download$3 or install$3 or upload$3 or send$3 or transmit$4) and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 14:30
-	226	((customize$1) adj3 (program or code or file)) same (download$3 or install$3 or upload$3 or send$3 or transmit$4) and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 14:32
-	0	((customize$1) adj3 (program or code or file)) same (download$3 or install$3 or upload$3 or send$3 or transmit$4) same (address near4 request)and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 14:33
-	16	((customize$1) adj3 (program or code or file)) same (download$3 or install$3 or upload$3 or send$3 or transmit$4) same (request)and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 14:33
-	15	(PLC or (automation adj device)) same (location) same (program$4 or software or code) same (download$4 or install$4 or upload$4) and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 14:42
-	1	(PLC or (automation adj device)) same (network with location) same (program$4 or software or code) same (download$4 or install$4 or upload$4 or transmit$4) and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 14:44
-	12	(PLC or (automat$4 adj device)) same (network with location) same (program$4 or software or code) same (download$4 or install$4 or upload$4 or transmit$4) and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 14:44
-	37	((automat$3 adj device) or (plc) or (logic adj controller)) same (request or message) same (download$3 or transmit$4 or install$3 or upload$3) same network and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 17:29
-	58	((automat$3 adj device) or (plc) or (logic adj controller)) same (request or message) same (download$3 or transmit$4 or install$3 or upload$3) same (program or software or instructions) and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 17:30
-	14	((automat$3 adj device) or (plc) or (logic adj controller)) same (request or message) same (download$3 or transmit$4 or install$3 or upload$3) near6 (program or software or instructions) and @ad<20000809	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/01 17:30

A customizable library to support software synthesis for embedded applications and micro-kernel systems

Full text Pdf (1.17 MB)

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Proceedings of the 8th ACM SIGOPS European workshop on Support for composing distributed applications table of contents
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Author Carsten Ditze

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Publisher ACM Press New York, NY, USA

↑ INDEX TERMS

Primary Classification:

D. Software
- **D.2** SOFTWARE ENGINEERING
  - **D.2.2** Design Tools and Techniques
    - **Subjects:** Software libraries

Additional Classification:

C. Computer Systems Organization
- **C.3** SPECIAL-PURPOSE AND APPLICATION-BASED SYSTEMS
  - **Subjects:** Real-time and embedded systems

D. Software
- **D.2** SOFTWARE ENGINEERING
  - **D.2.6** Programming Environments
    - **Subjects:** Programmer workbench
- **D.4** OPERATING SYSTEMS

S. K. Reinhardt, J. R. Larus, D. A. Wood
April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture**, Volume 22 Issue 2
Full text available: pdf(1.44 MB) Additional Information: full citation, abstract, references, citings, index terms

Future parallel computers must efficiently execute not only hand-coded applications but also programs written in high-level, parallel programming languages. Today's machines limit these programs to a single communication paradigm, either message-passing or shared-memory, which results in uneven performance. This paper addresses this problem by defining an interface, *Tempest*, that exposes low-level communication and memory-system mechanisms so programmers and compilers can customize polici ...

9 A customizable library to support software synthesis for embedded applications and micro-kernel systems
Carsten Ditze
September 1998 **Proceedings of the 8th ACM SIGOPS European workshop on Support for composing distributed applications**
Full text available: pdf(1.17 MB) Additional Information: full citation, index terms

10 Coherence controller architectures for SMP-based CC-NUMA multiprocessors
Maged M. Michael, Ashwini K. Nanda, Beng-Hong Lim, Michael L. Scott
May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture**, Volume 25 Issue 2
Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, references, citings, index terms

Scalable distributed shared-memory architectures rely on coherence controllers on each processing node to synthesize cache-coherent shared memory across the entire machine. The coherence controllers execute coherence protocol handlers that may be hardwired in custom hardware or programmed in a protocol processor within each coherence controller. Although custom hardware runs faster, a protocol processor allows the coherence protocol to be tailored to specific application needs and may shorten ha ...

11 Verification of electronic systems
Alberto L. Sangiovanni-Vincentelli, Patrick C. McGeer, Alexander Saldanha
June 1996 **Proceedings of the 33rd annual conference on Design automation conference**
Full text available: pdf(115.97 KB) Additional Information: full citation, references, citings, index terms

12 Development of processors and communication networks for embedded systems: Component-based design approach for multicore SoCs
W. Cesário, A. Baghdadi, L. Gauthier, D. Lyonnard, G. Nicolescu, Y. Paviot, S. Yoo, A. A. Jerraya, M. Diaz-Nava
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(187.82 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a high-level component-based methodology and design environment for application-specific multicore SoC architectures. Component-based design provides primitives to build complex architectures from basic components. This bottom-up approach allows design-architects to explore efficient custom solutions with best performances. This paper presents a high-level component-based methodology and design environment for